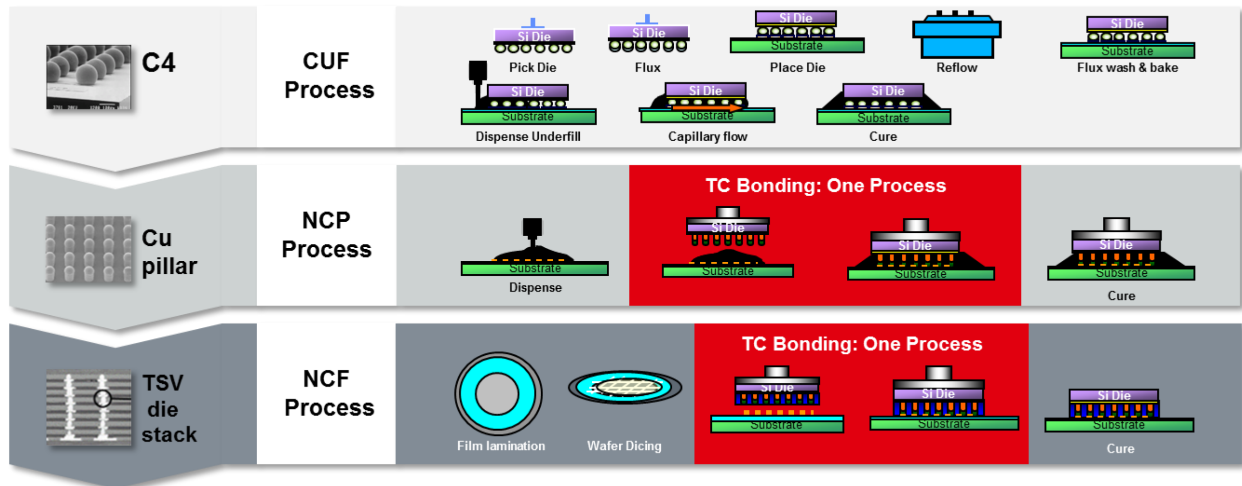
3D Packaging Technologies Benefit from Proven Underfill Protection to Secure Long-Term Reliability and Performance

Rose Guino, Ph.D. and Jie Bai, Ph.D.
Henkel Corporation

Mobile and computing technology have advanced at an accelerated pace over the last decade, with development and integration of various interconnect solutions enabling the rate of innovation. Historically, the most prevalent method for improving form and function has been transistor scaling, though new performance requirements have made this technique increasingly challenging and costly. In addition to transistor scaling and to achieve even greater cost and performance efficiencies, many device designers are considering new advanced packaging techniques to address the continued requirement for increased function and cost-effectiveness. Modern package designs include increased I/O, system-in-package, chiplets and higher interconnect densities, among others.

As newer packages become thinner and smaller with more I/O for greater function, ensuring the reliability of the designs becomes essential to long-term performance. Stress management and structural bump protection are critical factors, as chips are increasingly fragile with lower silicon nodes and ultra-low dielectric layers. Achieving higher functionality for a given die size has driven development of several approaches, one of which is copper (Cu) pillar technology. This technique places Cu pillar bumps in higher density, allowing for increased I/O and utilizing wafer functionality. But, like other challenging designs, Cu pillar bump pitches of less than 50 µm and narrow sub-40 µm bondline gaps make conventional bump protection methods increasingly problematic. Traditional capillary underfills (CUFs), for example, have difficulty flowing in and around the tight dimensions. Because flux cleaning under the tight spaces is also challenging, underfill compatibility with flux residues is a growing concern. For thinner wafers and dies with through silicon vias (TSVs) to accommodate 3D stacking, handling and warpage control is all the more challenging.

With this new technology landscape and the need to effectively protect delicate interconnects, non-conductive paste (NCP) and non-conductive film (NCF) – also referred to as wafer-applied underfill (WAUF) – materials have emerged as the most reliable underfill solutions for Cu pillar and TSV packaging approaches. Both NCP and NCF materials offer excellent bump-pad alignment accuracy through thermal compression bonding, as shown in the diagram below which compares capillary, paste and film processing steps.



In the memory market, however, where 3D TSV stacking applications have evolved into the dominant packaging technique, TSV die applications less than 50 µm thick are challenging for thermal compression bonding of paste materials. Because of the potential for die top and bonding tool contamination with NCPs, packaging specialists have moved toward the use of NCF for die structures – including TSV and Cu pillar -- where more controlled flow and precise fillet formation are required. As illustrated above, NCF is applied via lamination and not only protects the bumps on the wafer, but also serves as additional support for wafer handling and successive processing. Die stacking of NCF-protected TSV dies is highly viable and already well-proven in high volume manufacturing.

The latest NCF materials to be introduced to the market are wafer-applied underfill films from Henkel. Henkel's LOCTITE ABLESTIK NCF 200 series has been developed to facilitate die processing for die that are less than 50 µm thick and, as compared to previous generation materials, the new NCFs have a six-month shelf life when stored at 5°C and a long work life of eight weeks; six weeks at room temperature before lamination and an additional two weeks at room temperature after lamination of the wafer. The materials, which are customized by application with available thicknesses from 12 µm to 52 µm, have lower melt viscosities which allow for reduced bond force processing, exceptionally fast three-second cure, and no outgassing during processing. Henkel's NCF series films have been designed to balance flow behavior and cure kinetics to achieve good joints without entrapment or solder extrusion, provide good fillet coverage and complete gap filling.

In addition to all of the performance and reliability benefits afforded by NCF, film-based materials are ideal for the requirements of 3D TSV memory chip processing. Even for non-memory applications, the LOCTITE ABLESTIK NCF 200 series materials enable the close placement of multiple dies for SiP and heterogeneous integration designs, which is not achievable with paste-based materials. As the industry moves toward more challenging designs and 3D integration, advanced materials such as Henkel's new non-conductive films will be essential for robust wafer processing and long-term package reliability.

For more information about the benefits of NCF for advanced packaging processing, visit https://www.henkel-adhesives.com/us/en/industries/electronics/semiconductor-packaging.html and click on the ‘contact us’ link.”