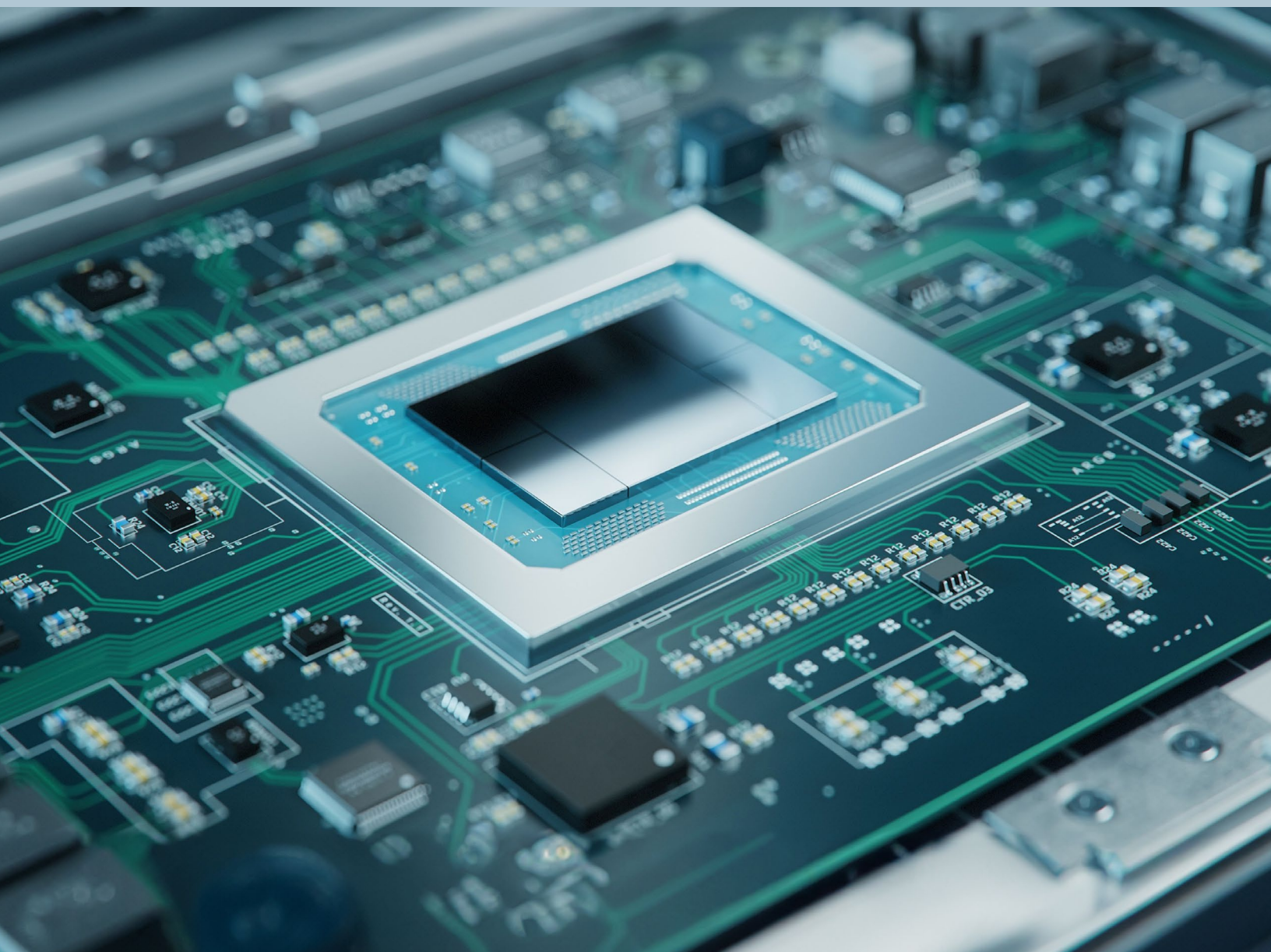
Henkel

Henkel Adhesive Technologies

ENSURING *LARGE DIE DURABILITY* IN **AI** AND **HPC** ADVANCED PACKAGES

Protection is Performance-Critical
Processability is Production-Vital



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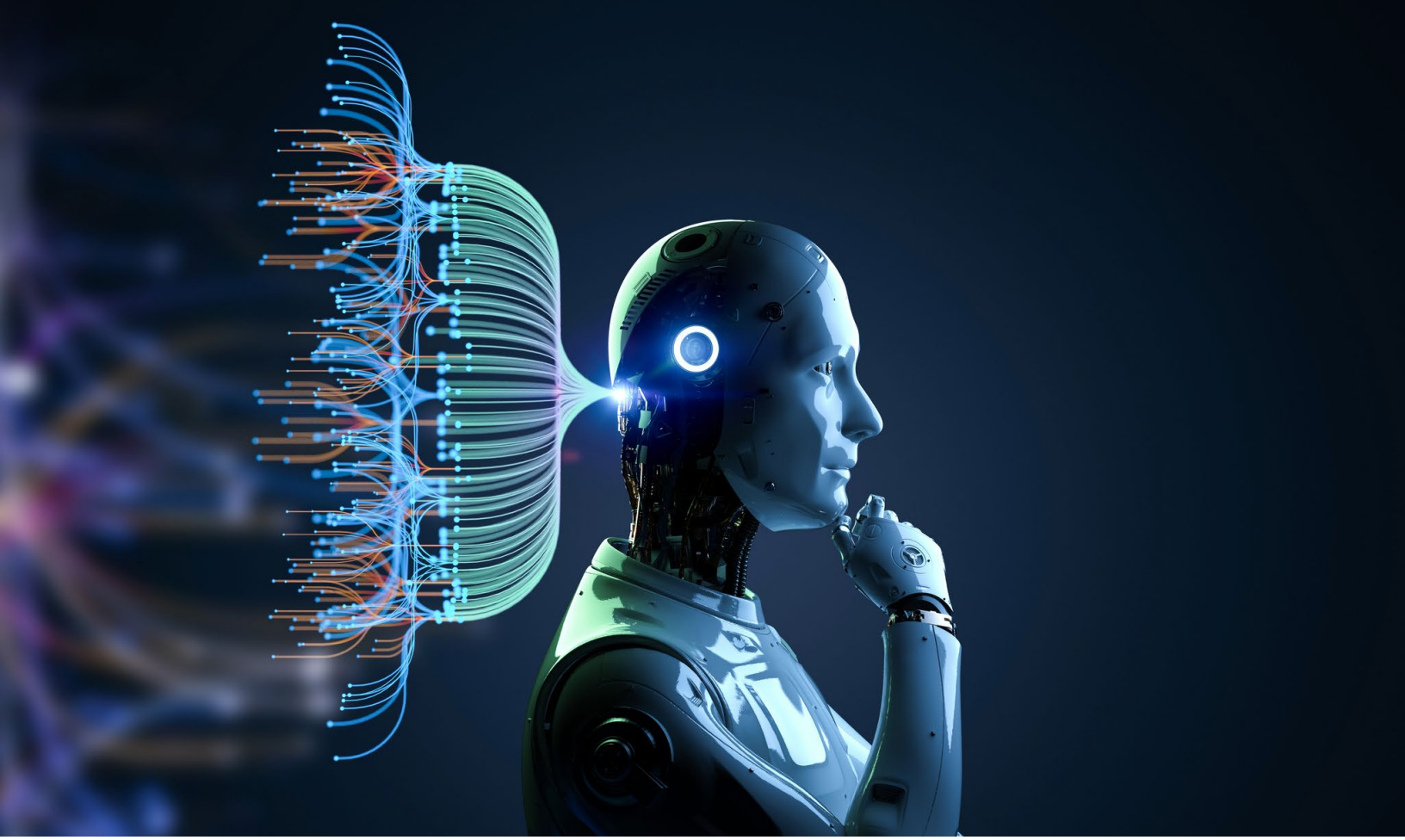


POWERFUL PACKAGES FUEL AI‘S SUCCESS

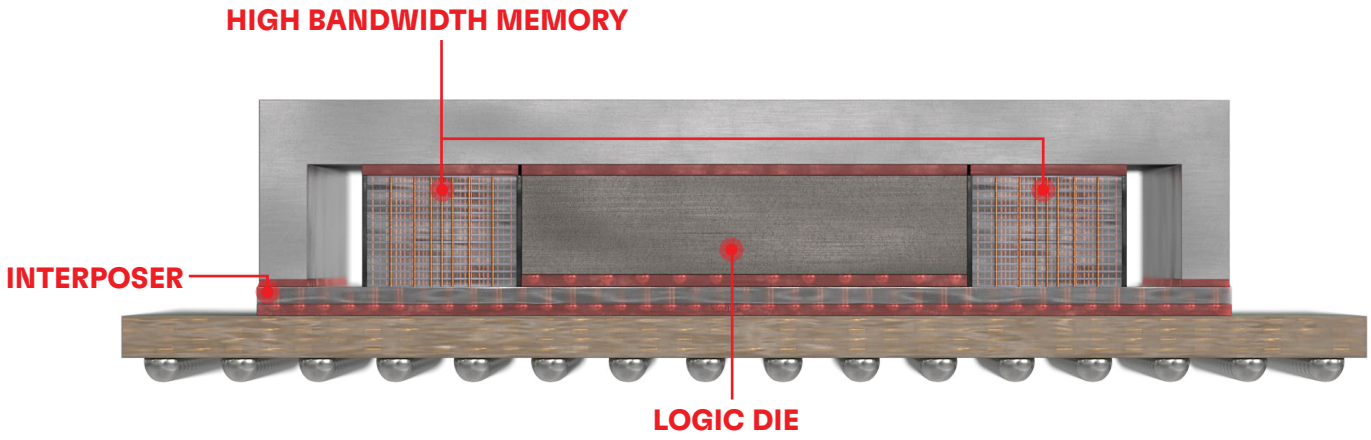
Nothing has illuminated the significance of advanced semiconductor packaging more than the data age and the recent, well-publicized growth of artificial intelligence (AI) and high-performance computing (HPC).

Though advanced packaging designs have been in use for decades, significant progress in **2.5D** and **3D heterogeneous integration** has been made over the last ten years to dramatically increase I/O, improve performance, realize cost-efficiencies, reduce power, and accelerate signal speeds for massive data processing.

> **Advanced packaging innovation is the primary enabler of powerful, high-bandwidth AI and HPC devices.**

COMPLEX LARGE BODY, LARGE DIE PACKAGES

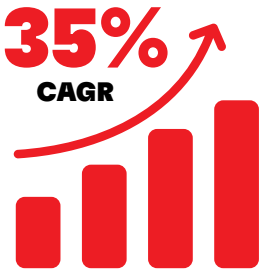
There is a diverse range of advanced packaging platforms, including fan-out wafer-level packaging/ 2.5-D, 3D stacked packaging, and system-on-a-chip (SoC). Several AI and HPC technologies leverage high-density fan-out HD-FO (or ultra-high-density fan-out)/2.5-D and 3D technologies, while other computing applications for servers, networking, gaming, and edge devices may use flip-chip BGA (FCBGA) designs. Next-generation **HD-FO/2.5-D packages** generally have sizeable footprints, integrating very large die. There are many examples of these designs -- such as **CoWoS®**, and **I-Cube®** – developed by the world's top semiconductor companies. While approaches and architectures vary, these technologies typically integrate a large interposer die/ redistribution layer (RDL) on which other die – logic, compute, and stacked high bandwidth memory – are integrated. The result is a sizeable package body, making processing and protection even more challenging.



Heterogeneous integration cross-section shows high bandwidth memory and logic dies integrated into one interposer, redistribution layer.

How big is big? The CoWoS (chip-on-wafer-on-substate) 2.5D platform, well-known in the AI and HPC GPU space, has seen several iterations. According to IEEE, the fifth generation of this technology may see CoWoS packages with interposers measuring **2500 mm²**.

There are many new HD-FO/2.5-D advanced packaging designs tackling the demands of AI and HPC which, according to market analyst Prismark, is a category that will see nearly **35% CAGR** over the next five years.



According to market analyst Prismark, HD-FO/2.5-D will see nearly 35% compound annual growth rate over the next five years.

With these new advanced packages, however, come challenges – particularly in relation to **ensuring the reliability of large – and getting larger –, high-density I/O die. Protecting against thermal-mechanical stress and die warpage for die of this scale while complying with processing demands is imperative.**

According to market analysts, the AI market leader‘s next GPU modules are going to be **big, powerful - and costly**! Some estimates put the price tag as **high as $100,000**.[1]

AS HIGH AS

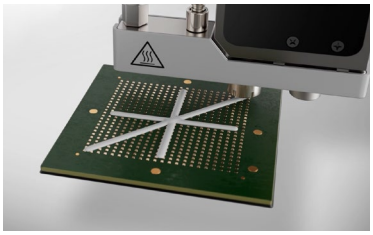
100K

[1] https://www.tomshardware.com/pc-components/gpus/nvidias-next-gen-ai-gpu-revealed-blackwell-b200-gpu-delivers-up-to-20-petaflops-of-compute-and-massive-improvements-over-hopper-h100

DIE PROTECTION IS VITAL TO PACKAGE RELIABILITY AND PERFORMANCE

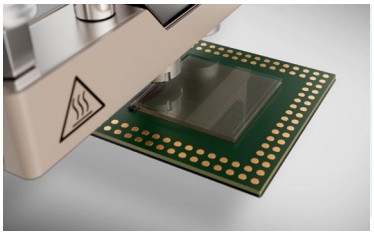
Underfill materials, introduced in the late 1990s to fortify PCB direct chip attach, are now essential for advanced semiconductor packaging to improve interconnect reliability. The epoxy-based materials protect against thermal-mechanical stress induced by coefficient of thermal expansion (CTE) variances between substrates and die. This capability **guards against factors like warpage and die cracking that can render an entire device inoperable**.

There are multiple package-level underfill formats:



NON-CONDUCTIVE PASTE

NON-CONDUCTIVE FILM



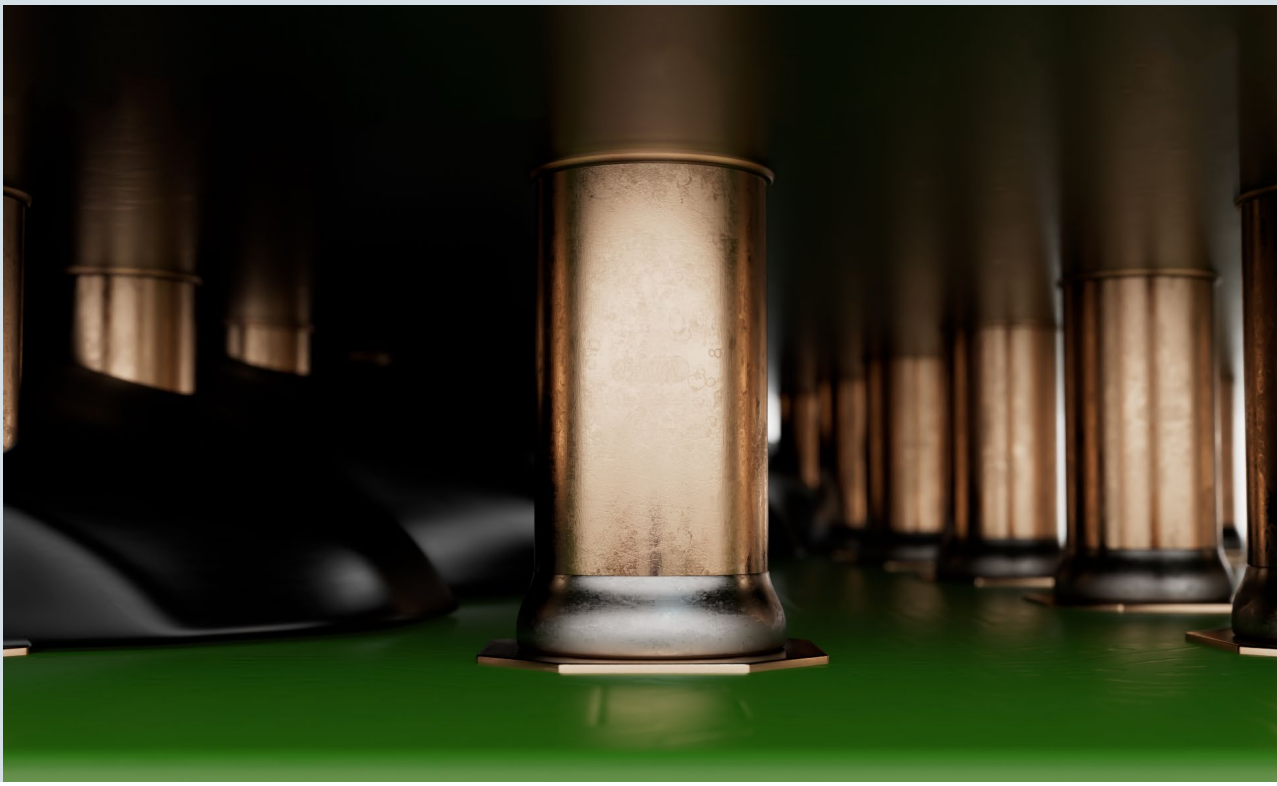
CAPILLARY

The effectiveness of various underfill types depends primarily on interconnect pitch, gap height, and processing preference. **Capillary flow underfills are preferred when it comes to HD-FO/2.5-D devices with bump pitches less than 100 µm and gap heights below 50 µm.**

The difficult – but critical – task of protecting large die (> 20 mm x 20 mm) I/O cannot be underestimated, and ensuring complete, void-free bump encapsulation using capillary flow underfills is challenging given the required coverage surface area and dimensional complexity.

The materials not only have to deliver the **adhesion, cured rigidness, high toughness**, and **crack resistance** required to secure die in-application, but must be formulated with a rheology **that enables fast flow, high UPH, and total die I/O coverage** before material gelation occurs.

Copper pillar interconnects with tight spacing and narrow gaps require underfills with fast, uniform flow capability.



FORMULATING FOR NEW DEVICE DIMENSIONS

An **underfill development project** to tackle the dimensional and processability obstacles associated with large die integration in AI and HPC devices was recently completed. A **balanced formulation** that meets the flow characteristics, low warpage, crack resistance, toughness, and long-term reliability performance required **for large die, flip chip BGA and Cu-pillar, highly integrated advanced semiconductor packages resulted in the development of LOCTITE® ECCOBOND UF 9000AE**. The material meets demanding metrics to enable current and next-generation large die advanced packages.

RHEOLOGY DESIGNED FOR THE UNIQUE CHARACTERISTICS OF LARGE, HIGH-DENSITY I/O DIE

Rheology optimization is one of the most challenging formulation aspects for large die capillary underfills. Rheological properties that enable the material to **flow quickly** within miniaturized interconnect pitch and gap dimensions for clean underfilling across a **large surface area** while providing high filler loading for maximum protection are essential. If the material flows too slowly, it may not only limit UPH, but can begin to gel before complete die interconnect coverage is achieved, adversely affecting reliability.

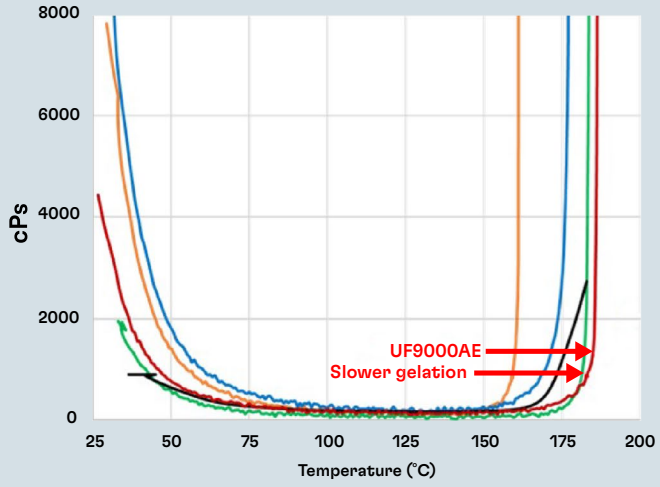
The new capillary underfill is a highly-filled material (~70% filler loading) that offers faster underfilling for more efficient **edge-to-edge die coverage**. In testing on die **as large as 40 mm x 40 mm with > 2,000 100 µm pitch bumps with 50 µm gap heights**, LOCTITE® ECCOBOND UF 9000AE demonstrated up to 20% faster flow* versus previous-generation materials.

The material has been verified on die as large as **50 mm x 50 mm** and its flow characteristics indicate compatibility with even larger die, supporting the evolution of HD-FO/2.5-D packaging. Importantly, this material's resin system limits resin bleed out (RBO) to enable the tight keep-out-zones necessary for highly integrated advanced packages.

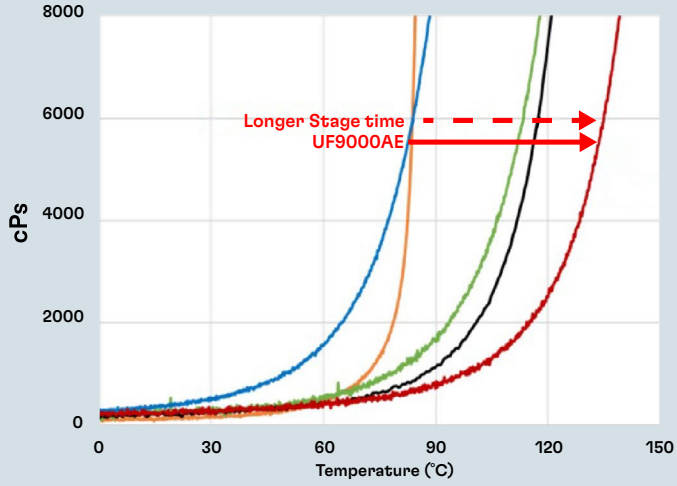
*Die size dependent.

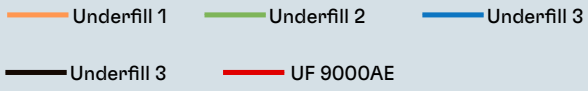
RHEOLOGICAL PROPERTIES OF LOCTITE® ECCOBOND UF 9000AE

Ramp Rheology



1000C Isothermal





As compared to previous-generation materials, LOCTITE® ECCOBOND UF 9000AE's rheological properties provide a longer stage time (up to 100 minutes) and slower gelation to enable complete bump encapsulation.

LOCTITE® ECCOBOND UF 9000AE prioritizes material reliability and complies with industry standards for operator safety. It contains no SVHCs under REACH regulations and does not contain any intentionally added PFAS, ensuring both quality and sustainability.

BUILT FOR BANDWIDTH: LOW STRESS, LOW WARPAGE, HIGH CRACK RESISTANCE

The most common failure mode within large die applications is die cracking, so formulating a material with properties optimized to prevent crack-related failures is critical for large die capillary underfills. With a low coefficient of thermal expansion (CTE) (23 ppm/°C below Tg), low modulus (13.5 GPa at 25°C), and a high K1c (3.0), LOCTITE® ECCOBOND UF 9000AE's material properties are well-balanced to address the challenges with die sizes measuring > 20 mm x 20 mm and as large as 50 mm x 50 mm. The formulation offers **a low-stress, lower warpage solution for large die**, significantly reducing the propensity for interconnect damage due to stressors like temperature differentials and warpage.

In testing versus other underfills, LOCTITE® ECCOBOND UF 9000AE showed higher fracture toughness and lower CTE and shrinkage, resulting in low stress on large die packages.

CRACK RESISTANCE OF LOCTITE® ECCOBOND UF 9000AE

High Fracture Toughness (K1c), CTE Improvement and Lower Shrinkage

Properties	Underfill 1	Underfill 2	LOCTITE® ECCOBOND UF 9000AE
Filler loading,%	60	50	68
Toughness (K1c), MPa√m	2.0	0.6	3.0
CTE1/CTE2, ppm/°C	25/100	30/119	23/84
Shrinkage, %	1.8	2.2	1.1

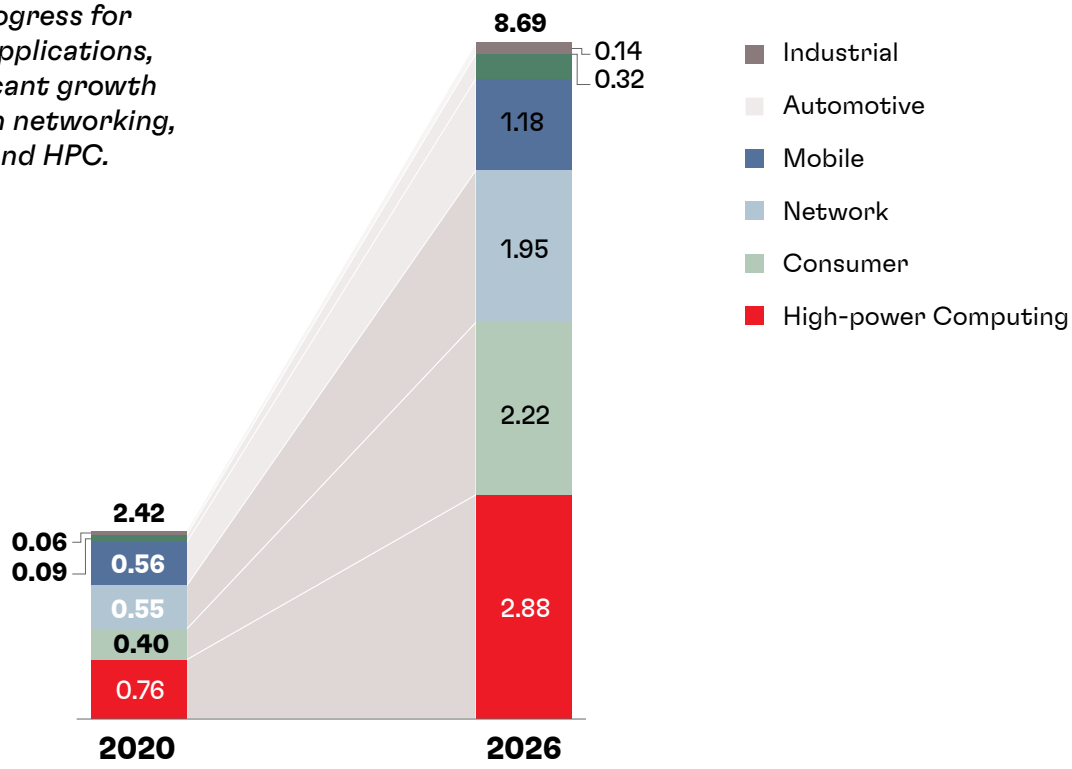
IT'S ADVANCED PACKAGING'S TIME TO SHINE

Thoroughly **protecting dense interconnects** across a large surface area is vital to advanced packaging's ability to **enable the market's most complex devices.** LOCTITE® ECCOBOND UF 9000AE is a notable achievement in this area and a proven contributor to overall package reliability and performance.

The advanced packaging market is spurred by end applications.[2]

Advanced packaging sales, by end application, $ billion

Advanced packaging is enabling progress for numerous applications, with significant growth projected in networking, consumer, and HPC.



While **advanced packaging** technologies have been around for almost **25 years**, their **most significant progress has come in the last decade.** With the catalyst of AI and HPC and the aid of continued material innovation, advanced packaging's influence is only projected to accelerate, making its **next decade perhaps the most impactful yet.**

[2] https://www.mckinsey.com/industries/semiconductors/our-insights/advanced-chip-packaging-how-manufacturers-can-play-to-win

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